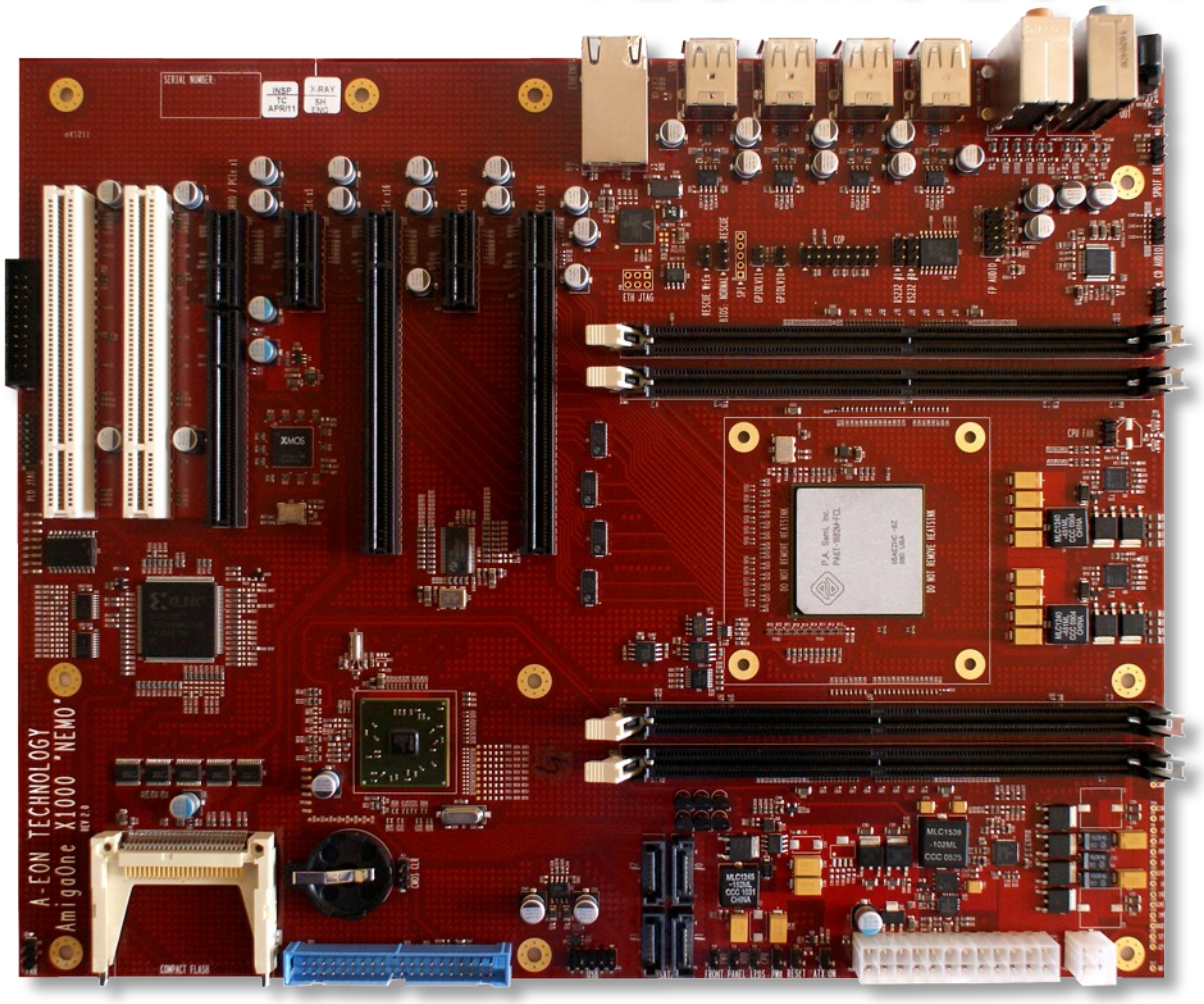
A-EON TECHNOLOGY



AmigaONE X1000

Nemo revision 2.1 Motherboard Technical Reference Manual

Version 1.5

December 13, 2011

FIRST CONTACT
AmigaOne X1000
Keep this party going

Document reference number TRM-NEMO-1.5

This document provides technical reference information for the Nemo motherboard developed by Varisys Ltd for and on behalf of A EON Technology for the AmigaOne X1000 computer, and is provided in confidence to members of the AmigaOne X1000 beta test team.

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1 Introduction

The Nemo motherboard combines a high performance PowerPC CPU with powerful and flexible I/O features to deliver the ultimate desktop platform for AmigaOS users.

This manual contains hardware and software reference information to assist with installation, configuration and low level programming of Nemo.

Please check with reseller for the latest recommendations on system components, including power supplies, DIMMs and PCIe/PCI cards.

For technical support, please contact your reseller.

2 Architecture

Nemo's architecture is shown in Figure 1 below:

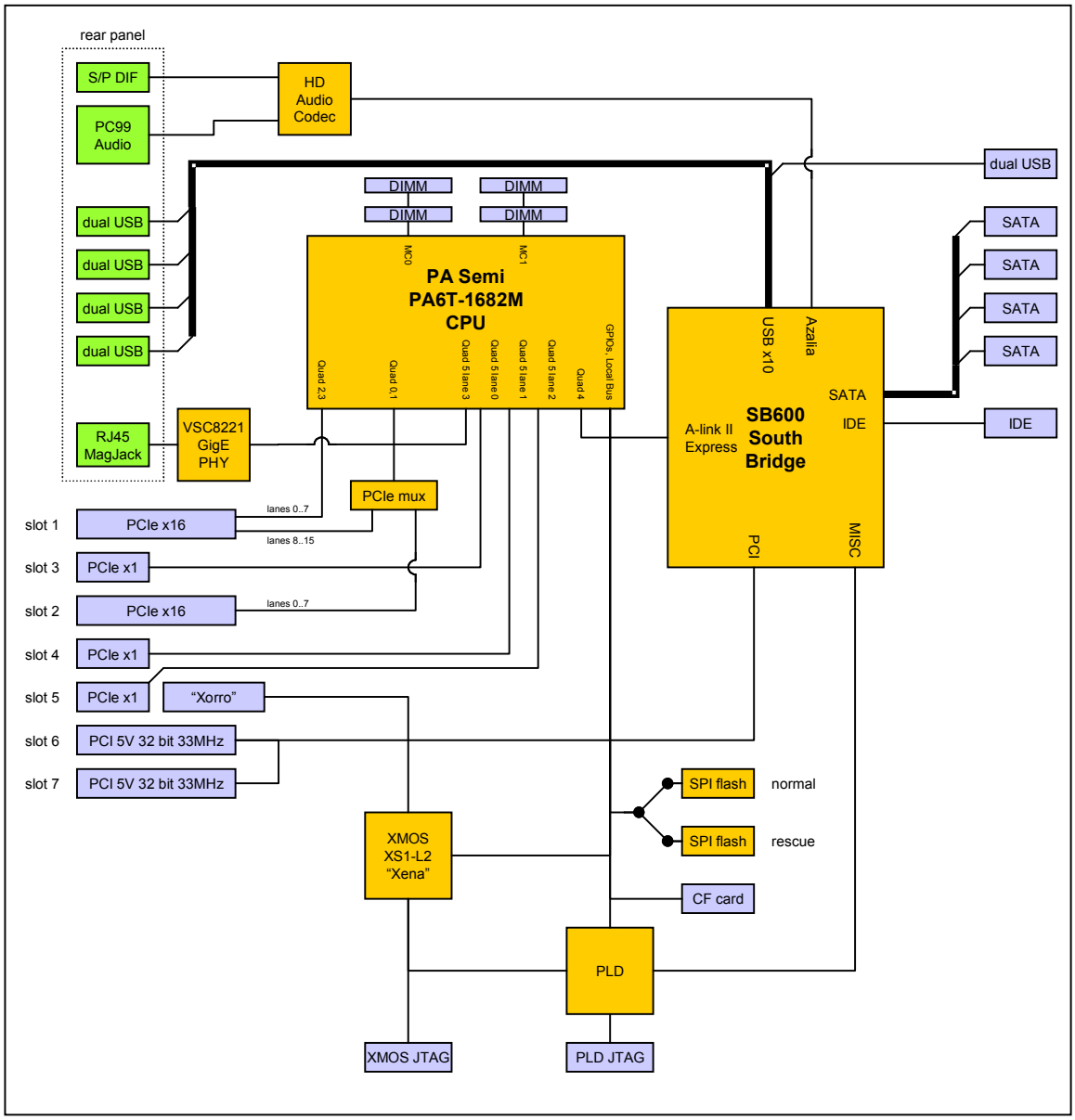

Figure 1: Nemo Motherboard Architecture

2.1 CPU

The CPU is a PA Semi "PWRficient" PA6T-1682M. This device combines dual 1.8GHz PowerPC cores with a 2MB L2 cache, dual channel DDR2 memory controllers and 24 SerDes channels.

The PowerPC cores adhere to the Power ISA v2.04, and support 64-bit extensions. They feature a double precision FPU and a VMX (AltiVec™) vector unit. They each have a 64kB I-cache and a 64kB D-cache.

The SerDes channels support PCI Express, XAUI and SGMII protocols. The "ENVOI" I/O subsystem which drives them includes caching, offload and DMA resources to maximise I/O performance.

For further details, see section 3.

2.2 Main Memory

The CPU memory controllers are each connected to a pair of standard DDR2 DIMM slots. For further details, see section 5.

2.3 South Bridge

The South Bridge is AMD/ATI's SB600, and provides the following I/O features:

- PCIe x4 link to CPU
- SATA-II AHCI controller with 4 ports
- PATA (IDE) controller (single channel)
- multiple USB ports
  - 5 OHCI and 1 EHCI host controllers
  - all ports are fully USB 1.1 and USB 2.0 compliant
- UAA compatible HD Audio controller
- PCIe-PCI bridge supporting multiple PCI slots with 5V signalling support
- 8259 compatible interrupt controller
- Real Time Clock

For further details, see section 4.

2.4 Ethernet

A single CPU SerDes channel is configured for SGMII protocol and this is connected to a Vitesse VSC8221 Gigabit Ethernet PHY. This is wired in turn to an RJ45 uplink connector at the rear.

2.5 "Xena"

An XMOS XS1-L2 "Software Defined Silicon" (SDS) device is provided to support simple, high performance I/O and a gateway to the parallel processing capabilities of XMOS technology.

For further details, see 6.

2.6 PCI and PCI Express Add-In Card Slots

Dual PCIe x16 slots are provided with automatic PCIe lane switching to support single or dual PCIe graphics cards. A further 3 x1 slots are also provided, as well as a pair of 32-bit 33MHz PCI slots suitable for 5V or universal cards.

Nemo complies with the relevant electromechanical specifications for these cards.

2.7 CompactFlash Card Slot

The CompactFlash (CF) card slot is wired to the CPU local bus. It is typically used to hold the operating system kernel.

2.8 BIOS

Dual serial flash EPROM chips are provided to hold the BIOS code. Jumpers are used to choose between them.

The BIOS code is maintained by Hyperion.

2.9 PLD

The PLD provides glue logic and control registers.

For further details, see section 7.

3 CPU

This section provides programmer visible details of CPU hardware implementation.

3.1 SerDes Lanes

The SerDes lanes are connected as shown in Table 1 below:

Quad	Lane	Connection
0	0	PCIe slot 1 lane 15 / PCIe slot 2 lane 7
0	1	PCIe slot 1 lane 14 / PCIe slot 2 lane 6
0	2	PCIe slot 1 lane 13 / PCIe slot 2 lane 5
0	3	PCIe slot 1 lane 12 / PCIe slot 2 lane 4
1	0	PCIe slot 1 lane 11 / PCIe slot 2 lane 3
1	1	PCIe slot 1 lane 10 / PCIe slot 2 lane 2
1	2	PCIe slot 1 lane 9 / PCIe slot 2 lane 1
1	3	PCIe slot 1 lane 8 / PCIe slot 2 lane 0
2	0	PCIe slot 1 lane 7
2	1	PCIe slot 1 lane 6
2	2	PCIe slot 1 lane 5
2	3	PCIe slot 1 lane 4
3	0	PCIe slot 1 lane 3
3	1	PCIe slot 1 lane 2
3	2	PCIe slot 1 lane 1
3	3	PCIe slot 1 lane 0
4	0	SB600 lane 0
4	1	SB600 lane 1
4	2	SB600 lane 2
4	3	SB600 lane 3
5	0	PCIe slot 3
5	1	PCIe slot 4
5	2	PCIe slot 5
5	3	Ethernet PHY

Table 1: CPU SerDes Lane Assignments

Notes:

1. The lanes associated with Quads 0 and 1 are steered to slot 2 if a card is present in that slot, otherwise they are steered to slot 1.
2. Quad 5 lane 3 is configured for SGMII, all others are PCIe.

3.2 Memory Controllers

The memory controllers are each wired to a pair of standard DDR2 DIMM sockets.

For further details, see section 5.

3.3 Local Bus

The local bus is wired to the SPI flash EPROMs, the PLD, the CompactFlash card and the XMOS device. Chip select assignments are shown in Table 2 below:

Chip Select	Width (bits)	Description
LB_CS_L[0]	16	CF card CS0#
LB_CS_L[1]	16	CF card CS1#
LB_CS_L[2]	n/a	not used
LB_CS_L[3]	n/a	not used
LB_CS_L[4]	8/16	Xena
LB_CS_L[5]	8	PLD
SPI_CS_L	n/a (SPI)	BIOS (SPI flash EPROM)

Table 2: CPU Local Bus Chip Selects

3.4 UARTs

The CPU provides dual UARTs. The UART receive and transmit signals are level shifted to RS232 levels, and provided on headers P26 and P27.

3.5 GPIOs

The CPU provides 16 general purpose I/Os (GPIOs). For details of how these are wired, see Table 3 below:

GPIO line	Signal Name	Direction	Connection	Notes
GPIO0	READY	in	CF card INTRQ	pulled up
GPIO1	VS1#	in	CF card VS1#	pulled up
GPIO2	LED_CPU	out	header P31	1 = on
GPIO3	SB600_IRQ	in	SB600 INTR	-
GPIO4	XMOS_IRQ#	in	XMOS X1D13	-
GPIO5	PHY_MDC	out	PHY MDC	-
GPIO6	PHY_MDIO	bidir	PHY MDIO	pulled up
GPIO7	PHY_IRQ#	in	PHY IRQ#	-
GPIO8	SMB_SEL0	out	SMbus 1:4 mux steering	see 3.6
GPIO9	SMB_SEL1	out	SMbus 1:4 mux steering	see 3.6
GPIOLV10	SJP2	in	JP2	0 = fitted
GPIOLV11	SJP3	in	JP3	0 = fitted
GPIOLV12	MC0_PERR	in	DIMM1,2 PAR_OUT	pulled up
GPIOLV13	MC1_PERR	in	DIMM3,4 PAR_OUT	pulled up
GPIOLV14	CFCD1	in	CF card CD1#	pulled up
GPIOLV15	CFCD2	in	CF card CD2#	pulled up

Table 3: CPU GPIOs

Note: a '#' suffix denotes an active-low signal.

3.6 SMbus Controllers

The CPU provides 3 SMbus controllers, and these are used to connect up various SMbus and I2C devices. The number of SMbusses is expanded to 7 via a 1:4 multiplexer on SMbus 1. SMbus wiring is detailed in Table 4 below:

Bus	Connection	Notes
0	peripherals & DIMM SPD	see below for peripheral details
1	SMbusses 3-6	via 1:4 mux
2	PCIe slot 1	
3	PCIe slot 2	from SMbus 1 via 1:4 mux
4	PCIe slot 3	from SMbus 1 via 1:4 mux
5	PCIe slot 4	from SMbus 1 via 1:4 mux
6	PCIe slot 5	from SMbus 1 via 1:4 mux

Table 4: CPU SMbus wiring

The steering of the 1:4 multiplexer on SMbus 1 is controlled by CPU GPIOs 8 and 9 as shown in Table 5 below:

GPIO9	GPIO8	SMbus connection
0	0	3
0	1	4
1	0	5
1	1	6

Table 5: SMbus multiplexing

SMbus 0 is connected to the 4 DIMM sockets to support Serial Presence Detect (SPD). For further details, see section 5. It is also connected to a standard 24LC128 EEPROM, and a temperature sensor (Texas Instruments TMP423). This sensor is connected to the CPU on-die temperature diodes for the 2 cores and SOC (main logic).

3.7 COP Header

The COP (debugger) header is provided for factory test purposes and its use is not recommended.

3.8 Core Supply

The CPU core supply is controlled by a MAX8720. VID codes must be set accordingly.

Warning: incorrect VID settings will permanently damage the CPU!

4 South Bridge

Nemo uses the AMD/ATI SB600 South Bridge to provide various integrated I/O functions including SATA/PATA ports, USB and audio.

Full details of this chip are available from AMD.

4.1 A-Link II Express

The SB600 connects to the CPU via a PCIe x4 link. This is termed an “A-link II Express” link by ATI/AMD for reasons that they are not keen to explain.

The design team determined early in the development of Nemo that the link’s behaviour as an endpoint does not comply fully with the PCI Express specification. Specifically, it requires the root complex to use non-zero device numbers in type 0 configuration cycles to enumerate all the devices within the SB600. This is related to the PC architecture and is used to allow SB600 devices appear on logical bus 0. A non-zero device number in a type 0 configuration cycle is normally illegal and most root complexes do not permit it, but PA Semi were kind enough to provide a register bit to relax this rule.

The more astute reader will deduce that the terse summary above conceals an epic saga of confusion, pain, and soaring triumph.

4.2 SATA and PATA (IDE)

SATA ports 0-3 are wired to headers J3-J6 respectively.

The PATA Controller is wired to header P6.

4.3 USB

The USB ports are wired to 8 USB A connectors on the back panel (P2-P5) and a header for front panel connection (P7).

A BD6512F-E2 current sensing power switch is used to monitor each pair of ports. The overcurrent sense signals for the 10 ports is wired to the SB600’s 10 overcurrent sense inputs (USB_OC0#-USB_OC9#).

4.4 HD Audio

The SB600’s HD Audio controller is connected to an IDT 92HD700 codec. This is wired to various audio connectors as follows:

- J7 = line in, mic in, and 7.1 out
- P15 = S/P DIF out (TOSlink optical)
- P16 = front panel audio
- P17 = CD audio in

Note that additional S/P DIF electrical connections are available although the use of these is not recommended (they are reserved for factory test):

- H5 = S/P DIF out
- P14 = S/P DIF in

4.5 Real Time Clock and CMOS Memory

A CR2032 type 3V coin cell is used to provide battery backup of the Real Time Clock and non-volatile (“CMOS”) memory. Jumper P11 may be used to clear the CMOS memory.

4.6 PCI Bus

The SB600 provides a PCI Express to PCI bridge. The PCI bus is wired to the PCI slots (6 and 7). The IDSEL and interrupt assignments for these slots are as shown in Table 6 below:

Slot	IDSEL	SB600 interrupt input			
		INTE#	INTF#	INTG#	INTH#
6	AD21	INTD#	INTA#	INTB#	INTC#
7	AD22	INTC#	INTD#	INTA#	INTB#

Table 6: PCI Slot IDSEL and Interrupt Wiring

4.7 Interrupt Controller

The 8259 interrupt controller INTR pin is wired to the CPU GPIO3.

The PCI interrupts INTA#-INTD# are wired to the SB600 external interrupt inputs INTE#-INTH#.

5 DIMMs

Nemo uses standard 1.8V DDR2 DIMMs, providing sockets for 2 on each memory controller for a total of 4.

The board has been qualified with unbuffered non-ECC DIMMs. For the latest information on recommended DIMM module types, please contact your reseller.

5.1 Interleaving

If both memory controllers are used, the memory population on each should exactly match (the modules fitted to DIMM1 and DIMM2 should exactly match the modules fitted to DIMM3 and DIMM4). This allows the memory controllers to be interleaved, effectively doubling memory bandwidth.

5.2 Size

It is theoretically possible to populate each memory controller with 8GB for a total of 16GB, however the practical memory size limit will depend on software.

5.3 Speed

The maximum speed supported by the memory controllers is DDR2-800. Faster memory may be fitted but this speed limit will apply.

5.4 Serial Presence Detect

The Serial Presence Detect (SPD) address of the 4 DIMM sockets is as shown in Table 7 below:

Socket	SA2	SA1	SA0
DIMM1	0	0	0
DIMM2	0	0	1
DIMM3	0	1	0
DIMM4	0	1	1

Table 7: SIMM SPD Addresses

6 Xena

Nemo includes direct support for XMOS “SDS” (Software Defined Silicon) technology. A dedicated XMOS device, designated “Xena”, is provided on-board.

Xena is connected to both the main CPU and a custom expansion slot (“Xorro”), which is mechanically aligned with a conventional PCI Express x1 slot.

Xorro expansion cards may be enhanced by adding connectivity to the PCI Express bus. Alternatively, if the Xorro slot is not required, the PCI Express slot connector can be used for conventional PCI Express x1 add-in cards.

This section provides implementation details of the Xena subsystem, and should be read in conjunction with relevant XMOS documentation.

6.1 Block Diagram

Figure 2 shows how Xena is connected to the main processor, the PLD, the XTAG debug header and the Xorro slot:

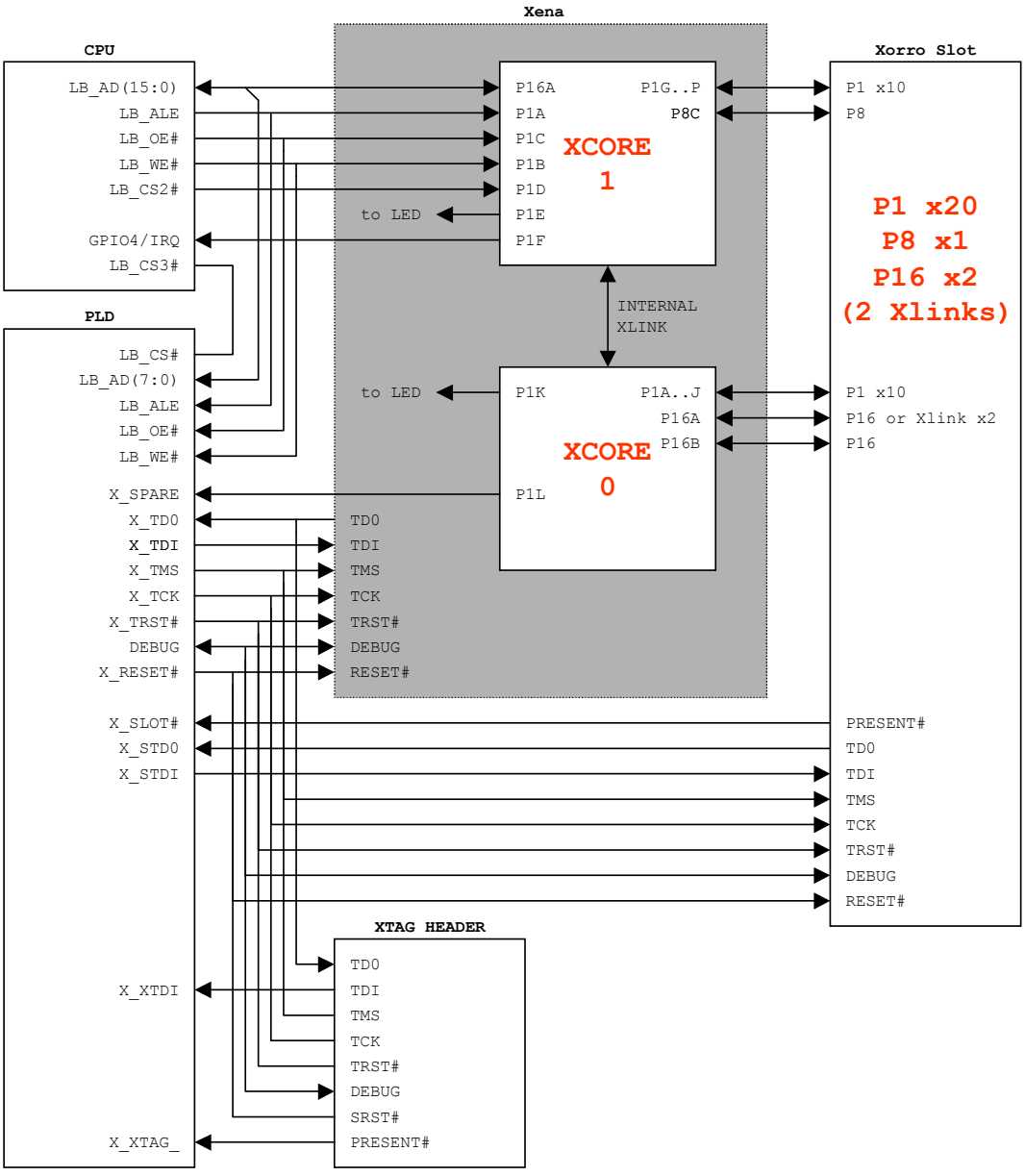

Figure 2: XMOS Subsystem Block Diagram

6.2 XMOS Device Type and Clocking

Xena is a 500MHz, dual-core XS1-L2, in a 124-pin QFN package. It is clocked from a 25MHz oscillator, and its PLL is configured for x20 operation i.e. a core clock speed of 500MHz.

6.3 Bootstrapping and Debug

Bootstrapping and debug of Xena is accomplished via its reset, JTAG and debug signals. These are connected to the PLD, and may be controlled and sampled via either an XTAG debugger (if fitted) or via PLD registers (see section 7 for details of these).

The Xena chip will be the only device on the JTAG chain unless a Xorro card with JTAG devices is fitted. In this case, the PLD will route the JTAG chain through the Xorro card first, so that any devices on it will appear earlier in the chain (Xorro's TDO connects to Xena's TDI).

Xena's control and debug signals are also connected to a header to allow the use of an XMOS XTAG debugger. If one is connected, the PLD will float most of its pins, allowing the XTAG to take over. It will, however, still provide automatic routing of the TDI/TDO signal chain through a Xorro card, if required, so that the XTAG can control both Xena and Xorro together.

6.4 CPU Local Bus

As shown in Figure 2, a number of ports from Xcore 1 are connected to the CPU local bus. The intention is that a thread on Xcore 1 should be programmed to emulate an 8- or 16-bit static memory device with multiplexed address/data, and to act as a conduit for data transfers between the CPU and other threads/cores.

6.5 Xorro Slot

The Xorro slot connector is physically a PCI Express x8 (98 pin) card edge connector. Xorro cards are not compatible with PCI Express x8 cards. The pinout of the Xorro slot connector is provided in section 8, together with signal descriptions.

6.6 LEDs

A pair of simple LEDs is provided for diagnostic purposes. These are connected to Xcore 0 (port P1K) and Xcore 1 (port P1E), and are illuminated when driven low.

6.7 Spare Port Line

The spare port line (Xcore 0 port P1L) is connected to the PLD. Its use is reserved. It should be tristated.

6.8 PCU

Xena's PCU (Power Control Unit) is not used.

7 PLD

A Xilinx XC2C128 PLD is used to provide glue logic and simple control registers.

7.1 Registers

The registers are presented at byte offsets in chip select 5 of the CPU local bus, as detailed in Table 8 below:

Offset	Name	R/W	Notes
0x0	VER_PLD	R	PLD version (4)
0x1	VER_PCB	R	0x10 = rev 1.0, 0x20 = for rev 2.0/2.1
0x2	SCRATCH	R/W	8 bit scratchpad
0x3	SLOT2	R	bit 0 = 1 if a card is present in slot 2
0x4	ALIVE	R/W	bit 0 is set to 1 by the CPU to indicate to the PLD that it has booted; this can be used in power/reset sequencing logic (but is not)
0x7	SPBTN	R/W	soft power button: writing 1 to bit 0 has the same effect as holding the power button; this will cause the board to power down after a few seconds
0x8	LBLED	R/W	write 1 to bit 0 to illuminated LED
0xC	XCTRL	R/W	0: RESET (write 1 to assert) 1: DEBUG in state (read only) 2: DEBUG out state 3: DEBUG out enable (1 = enabled) 6: Xorro card detect (1 = present) 7: XTAG detect (1 = present)
0xD	XJTAG	R/W	0: TCK 1: TMS 2: TDI 3: TDO (read only) 4: TRST (0 = negated/high, 1 = asserted/low)

Table 8: PLD Registers

All address offsets and bit positions not mentioned are reserved. For reserved bits, always write 0, and read values are undefined.

7.2 Programming Header

A header is provided to support programming of the PLD via a standard Xilinx adapter. This is reserved for factory test.

8 Connectors, Switches, Jumpers and LEDs

8.1 Switches

Headers are provided for front panel power and reset switches/buttons of the momentary, normally open type. P33 (labelled PWR) is for the power button. P36 (labelled RESET) is for the reset button. For both of these, pin 1 is grounded and pin 2 is pulled up to 3.3V.

8.2 Jumpers

8.2.1 BIOS Flash Selection

JP1 is used to select which flash EPROM is used for CPU booting. In postion 1-2, it selects the normal flash image. In position 2-3 it selects the rescue flash image.

> *Note that it is possible to corrupt the rescue flash image. This jumper should only ever be moved to position 2-3 in an emergency, and instructions for recovering the normal flash image should be followed with great care.*

8.2.2 GPIOLV

JP2 controls the state of CPU GPIOLV10 which is pulled up. Fitting a jumper causes the signal to be grounded. JP3 does the same for CPU GPIOLV11.

8.2.3 CMOS Clear

To clear the CMOS RAM, fit a jumper link to P11 pins 2-3 momentarily before returning it to pins 1-2 for normal operation.

8.3 LEDs

Nemo provides 6 on-board LEDs and headers for 3 external LEDs, detailed in Table 9 below:

Reference	Type	Description
LED1	0805, red	general power supply fault
LED2	0805, red	CPU core supply fault
LED3	0805, red	SB600 power good (PLD controlled)
LED4	0805, red	CPU power good (PLD controlled)
LED5	0805, red	SB600 running (PLD controlled)
LED6	0805, red	local bus LED register (PLD controlled)
P29	0.2" header	power on
P30	0.1" header	SATA/PATA(IDE) activity
P31	0.1" header	CPU GPIO2

Table 9: LEDs

Notes:

1. The LED header drivers are of the constant current (20mA) type and are suitable for driving LEDs with a forward voltage of between 2V and 12V.
2. P29 is pinned out as follows: 1,2 = +/anode, 3 = -/cathode. P30 and P31 are pinned out as follows: 1 = +/anode, 2 = -/cathode. Pin 1 is marked by an arrow in each case.

8.4 RS232

The pinouts of the 2 RS232 headers (P26, P27) are shown in Table 10:

These connectors are labelled “RS232 #0” and “RS232 #1” respectively.

Pin	Signal
1	Ground
2	TX (output from board)
3	RX (input to board)

Table 10: RS232 Header Pinout

8.5 DIMMs

The pinouts of the 4 DIMM sockets (DIMM1-DIMM4) are shown in Table 11:

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VREF	61	A4	121	VSS	181	+1.8V
2	VSS	62	+1.8V	122	DQ4	182	A3
3	DQ0	63	A2	123	DQ5	183	A1
4	DQ1	64	+1.8V	124	VSS	184	+1.8V
5	VSS	65	VSS	125	DM0	185	CK0_p
6	DQS0_n	66	VSS	126	n/c	186	CK0_n
7	DQS0_p	67	+1.8V	127	VSS	187	+1.8V
8	VSS	68	PAR_IN	128	DQ6	188	A0
9	DQ2	69	+1.8V	129	DQ7	189	+1.8V
10	DQ3	70	A10/AP	130	VSS	190	BA1
11	VSS	71	BA0	131	DQ12	191	+1.8V
12	DQ8	72	+1.8V	132	DQ13	192	RAS#
13	DQ9	73	WE#	133	VSS	193	S0#
14	VSS	74	CAS#	134	DM1	194	+1.8V
15	DQS1_n	75	+1.8V	135	n/c	195	ODT0
16	DQS1_p	76	S1#	136	VSS	196	A13
17	VSS	77	ODT1	137	CK1_p	197	+1.8V
18	RESET#	78	+1.8V	138	CK1_n	198	VSS
19	n/c	79	VSS	139	VSS	199	DQ36
20	VSS	80	DQ32	140	DQ14	200	DQ37
21	DQ10	81	DQ33	141	DQ15	201	VSS
22	DQ11	82	VSS	142	VSS	202	DM4
23	VSS	83	DQS4_n	143	DQ20	203	n/c
24	DQ16	84	DQS4_p	144	DQ21	204	VSS
25	DQ17	85	VSS	145	VSS	205	DQ38
26	VSS	86	DQ34	146	DM2	206	DQ39
27	DQS2_n	87	DQ35	147	n/c	207	VSS
28	DQS2_p	88	VSS	148	VSS	208	DQ44
29	VSS	89	DQ40	149	DQ22	209	DQ45
30	DQ18	90	DQ41	150	DQ23	210	VSS
31	DQ19	91	VSS	151	VSS	211	DM5
32	VSS	92	DQS5_n	152	DQ28	212	n/c
33	DQ24	93	DQS5_p	153	DQ29	213	VSS
34	DQ25	94	VSS	154	VSS	214	DQ46
35	VSS	95	DQ42	155	DM3	215	DQ47
36	DQS3_n	96	DQ43	156	n/c	216	VSS
37	DQS3_p	97	VSS	157	VSS	217	DQ52
38	VSS	98	DQ48	158	DQ30	218	DQ53
39	DQ26	99	DQ49	159	DQ31	219	VSS
40	DQ27	100	VSS	160	VSS	220	CK2_p
41	VSS	101	SA2	161	CB4	221	CK2_n
42	CB0	102	n/c	162	CB5	222	VSS
43	CB1	103	VSS	163	VSS	223	DM6
44	VSS	104	DQS6_n	164	DM8	224	n/c
45	DQS8_n	105	DQS6_p	165	n/c	225	VSS
46	DQS8_p	106	VSS	166	VSS	226	DQ54
47	VSS	107	DQ50	167	CB6	227	DQ55
48	CB2	108	DQ51	168	CB7	228	VSS
49	CB3	109	VSS	169	VSS	229	DQ60
50	VSS	110	DQ56	170	+1.8V	230	DQ61
51	+1.8V	111	DQ57	171	CKE1	231	VSS
52	CKE0	112	VSS	172	+1.8V	232	DM7
53	+1.8V	113	DQS7_n	173	A15	233	n/c
54	BA2	114	DQS7_p	174	A14	234	VSS
55	PAR_OUT	115	VSS	175	+1.8V	235	DQ62
56	+1.8V	116	DQ58	176	A12	236	DQ63
57	A11	117	DQ59	177	A9	237	VSS
58	A7	118	VSS	178	+1.8V	238	+3.3V
59	+1.8V	119	SDA	179	A8	239	SA0
60	A5	120	SCL	180	A6	240	SA1

Table 11: DIMM Socket Pinout

8.6 CompactFlash Card Slot

The pinout of the CompactFlash card slot is shown in Table 12:

Pin	Signal	Pin	Signal
1	GND	26	CD1#
2	D03	27	D11
3	D04	28	D12
4	D05	29	D13
5	D06	30	D14
6	D07	31	D15
7	CS0#	32	CS1#
8	A10	33	VS1#
9	OE#	34	IORD#
10	A09	35	IOWR#
11	A08	36	WE#
12	A07	37	READY
13	+3.3V	38	+3.3V
14	A06	39	CSEL
15	A05	40	VS2#
16	A04	41	RESET
17	A03	42	IORDY
18	A02	43	INPACK
19	A01	44	REG
20	A00	45	DASP
21	D00	46	PDIAG
22	D01	47	D08
23	D02	48	D09
24	WP	49	D10
25	CD2#	50	GND

Table 12: CompactFlash Card Slot Pinout

Note: a '#' suffix signifies an active low signal.

8.7 PCIe and PCI Slots

The pinout of the slots 1 and 2 is shown in Table 13. The pinout of slots 3, 4 and 5 is shown in Table 14. The pinout of slots 6 and 7 is shown in Table 15.

Note: a '#' suffix signifies an active low signal.

pin	row A	row B	pin	row A	row B
1	PRSNT1#	+12V	42	GND	PETn6
2	+12V	+12V	43	PERp6	GND
3	+12V	+12V	44	PERn6	GND
4	GND	GND	45	GND	PETp7
5	TCK	SMCLK	46	GND	PETn7
6	TDI	SMDAT	47	PERp7	GND
7	TDO	GND	48	PERn7	PRSNT2#
8	TMS	+3.3V	49	GND	GND
9	+3.3V	TRST#	50	RSVD	PETp8
10	+3.3V	3.3Vaux	51	GND	PETn8
11	PERST#	WAKE#	52	PERp8	GND
12	GND	RSVD	53	PERn8	GND
13	REFCLK+	GND	54	GND	PETp9
14	REFCLK-	PETp0	55	GND	PETn9
15	GND	PETn0	56	PERp9	GND
16	PERp0	GND	57	PERn9	GND
17	PERn0	PRSNT2#	58	GND	PETp10
18	GND	GND	59	GND	PETn10
19	RSVD	PETp1	60	PERp10	GND
20	GND	PETn1	61	PERn10	GND
21	PERp1	GND	62	GND	PETp11
22	PERn1	GND	63	GND	PETn11
23	GND	PETp2	64	PERp11	GND
24	GND	PETn2	65	PERn11	GND
25	PERp2	GND	66	GND	PETp12
26	PERn2	GND	67	GND	PETn12
27	GND	PETp3	68	PERp12	GND
28	GND	PETn3	69	PERn12	GND
29	PERp3	GND	70	GND	PETp13
30	PERn3	RSVD	71	GND	PETn13
31	GND	PRSNT2#	72	PERp13	GND
32	RSVD	GND	73	PERn13	GND
33	RSVD	PETp4	74	GND	PETp14
34	GND	PETn4	75	GND	PETn14
35	PERp4	GND	76	PERp14	GND
36	PERn4	GND	77	PERn14	GND
37	GND	PETp5	78	GND	PETp15
38	GND	PETn5	79	GND	PETn15
39	PERp5	GND	80	PERp15	GND
40	PERn5	GND	81	PERn15	PRSNT2#
41	GND	PETp6	82	GND	RSVD

Table 13: PCIe x16 Slot Pinout

Note: Slot 1 lanes 8-15 are no connect if a card is present in slot 2. Slot 2 lanes 8-15 are always no connect.

pin	Row A	Row B
1	PRSNT1#	+12V
2	+12V	+12V
3	+12V	+12V
4	GND	GND
5	TCK	SMCLK
6	TDI	SMDAT
7	TDO	GND
8	TMS	+3.3V
9	+3.3V	TRST#
10	+3.3V	3.3VAUX
11	PERST#	WAKE#
12	GND	RSVD
13	REFCLK+	GND
14	REFCLK-	PETp0
15	GND	PETn0
16	PERp0	GND
17	PERn0	PRSNT2#
18	GND	GND

Table 14: PCIe x1 Slot Pinout

pin	Row A	Row B	pin	Row A	Row B
1	TRST#	-12V	32	AD[16]	AD[17]
2	+12V	TCK	33	+3.3V	C/BE[2]#
3	TMS	GND	34	FRAME#	GND
4	TDI	TDO	35	GND	IRDY#
5	+5V	+5V	36	TRDY#	+3.3V
6	INTA#	+5V	37	GND	DEVSEL#
7	INTC#	INTB#	38	STOP#	GND
8	+5V	INTD#	39	+3.3V	LOCK#
9	RSVD	PRSNT1#	40	RSVD	PERR#
10	+5V	RSVD	41	RSVD	+3.3V
11	RSVD	PRSNT2#	42	GND	SERR#
12	GND	GND	43	PAR	+3.3V
13	GND	GND	44	AD[15]	C/BE[1]#
14	3.3VAUX	RSVD	45	+3.3V	AD[14]
15	RST#	GND	46	AD[13]	GND
16	+5V	CLK	47	AD[11]	AD[12]
17	GNT#	GND	48	GND	AD[10]
18	GND	REQ#	49	AD[09]	GND
19	PME#	+5V	50	-KEY-	-KEY-
20	AD[30]	AD[31]	51	-KEY-	-KEY-
21	+3.3V	AD[29]	52	C/BE[0]#	AD[08]
22	AD[28]	GND	53	+3.3V	AD[07]
23	AD[26]	AD[27]	54	AD[06]	+3.3V
24	GND	AD[25]	55	AD[04]	AD[05]
25	AD[24]	+3.3V	56	GND	AD[03]
26	IDSEL	C/BE[3]#	57	AD[02]	GND
27	+3.3V	AD[23]	58	AD[00]	AD[01]
28	AD[22]	GND	59	+5V	+5V
29	AD[20]	AD[21]	60	REQ64#	ACK64#
30	GND	AD[19]	61	+5V	+5V
31	AD[18]	+3.3V	62	+5V	+5V

Table 15: PCI Slot Pinout

8.8 Xena Connectors

The pinout of the Xorro slot is shown in Table 16 and Table 17 below. See Table 18 for signal descriptions. The pinout of the XTAG (XMOS JTAG) header is shown in Table 19.

Pin	Signal	Xcore	Ports				Links	
			1 bit	*4 bit*	*8 bit*	*16 bit*	*5 bit*	*2 bit*
A1	PRESENT#							
A2	3.3V							
A3	GND							
A4	CLK							
A5	GND							
A6	DEBUG							
A7	RESET#							
A8	reserved							
A9	3.3V							
A10	GND							
A11	5V							
A12	GND							
A13	X0D1	0	P1B0				XLA4out	
A14	X0D11	0	P1D0					
A15	X0D13	0	P1F0				XLB4out	
A16	GND							
A17	X0D14	0		P4C0	P8B0	P16A8	XLB3out	
A18	X0D15	0		P4C1	P8B1	P16A9	XLB2out	
A19	X0D16	0		P4D0	P8B2	P16A10	XLB1out	XLB1out
A20	X0D17	0		P4D1	P8B3	P16A11	XLB0out	XLB0out
A21	X0D18	0		P4D2	P8B4	P16A12	XLB0in	XLB0in
A22	X0D19	0		P4D3	P8B5	P16A13	XLB1in	XLB1in
A23	X0D20	0		P4C2	P8B6	P16A14	XLB2in	
A24	X0D21	0		P4C3	P8B7	P16A15	XLB3IN	
A25	GND							
A26	X0D23	0	P1H0					
A27	X0D25	0	P1J0					
A28	GND							
A29	X0D36	0	P1M0		P8D0	P16B8		
A30	X0D37	0	P1N0		P8D1	P16B9		
A31	X0D38	0	P1I0		P8D2	P16B10		
A32	X0D39	0	P1P0		P8D3	P16B11		
A33	X0D40	0			P8D4	P16B12		
A34	X0D41	0			P8D5	P16B13		
A35	X0D42	0			P8D6	P16B14		
A36	X0D43	0			P8D7	P16B15		
A37	GND							
A38	X1D23	1	P1H0					
A39	X1D25	1	P1J0					
A40	GND							
A41	X1D30	1		P4F2	P8C4	P16B4		
A42	X1D31	1		P4F3	P8C5	P16B5		
A43	X1D32	1		P4E2	P8C6	P16B6		
A44	X1D33	1		P4E3	P8C7	P16B7		
A45	GND							
A46	X1D35	1	P1L0					
A47	X1D37	1	P1N0		P8D1	P16B9		
A48	X1D39	1	P1P0		P8D3	P16B11		
A49	GND							

Table 16: Xorro Slot Pinout - A row

Pin	Signal	Xcore	Ports				Links	
			1 bit	*4 bit*	*8 bit*	*16 bit*	*5 bit*	*2 bit*
B1	GND							
B2	3.3V							
B3	TRST#							
B4	GND							
B5	TCK							
B6	TMS							
B7	TDI							
B8	TDO							
B9	3.3V							
B10	GND							
B11	5V							
B12	GND							
B13	X0D0	0	P1A0					
B14	X0D10	0	P1C0				XLA4in	
B15	X0D12	0	P1E0					
B16	GND							
B17	X0D2	0		P4A0	P8A0	P16A0	XLA3out	
B18	X0D3	0		P4A1	P8A1	P16A1	XLA2out	
B19	X0D4	0		P4B0	P8A2	P16A2	XLA1out	XLA1out
B20	X0D5	0		P4B1	P8A3	P16A3	XLA0out	XLA0out
B21	X0D6	0		P4B2	P8A4	P16A4	XLA0in	XLA0in
B22	X0D7	0		P4B3	P8A5	P16A5	XLA1in	XLA1in
B23	X0D8	0		P4A2	P8A6	P16A6	XLA2in	
B24	X0D9	0		P4A3	P8A7	P16A7	XLA3IN	
B25	GND							
B26	X0D22	0	P1G0				XLB4in	
B27	X0D24	0	P1I0					
B28	GND							
B29	X0D26	0		P4E0	P8C0	P16B0		
B30	X0D27	0		P4E1	P8C1	P16B1		
B31	X0D28	0		P4F0	P8C2	P16B2		
B32	X0D29	0		P4F1	P8C3	P16B3		
B33	X0D30	0		P4F2	P8C4	P16B4		
B34	X0D31	0		P4F3	P8C5	P16B5		
B35	X0D32	0		P4E2	P8C6	P16B6		
B36	X0D33	0		P4E3	P8C7	P16B7		
B37	GND							
B38	X1D22	1	P1G0				XLB4in	
B39	X1D24	1	P1I0					
B40	GND							
B41	X1D26	1		P4E0	P8C0	P16B0		
B42	X1D27	1		P4E1	P8C1	P16B1		
B43	X1D28	1		P4F0	P8C2	P16B2		
B44	X1D29	1		P4F1	P8C3	P16B3		
B45	GND							
B46	X1D34	1	P1K0					
B47	X1D36	1	P1M0		P8D0	P16B8		
B48	X1D38	1	P1I0		P8D2	P16B10		
B49	GND							

Table 17: Xorro Slot Pinout - B row

Signal Name(s)	Direction	Description	Card Design Notes
XnDn	I/O	XMOS port/link signals	
PRESENT#	O	card presence detect	connect to ground
RESET#	I	Reset, as used by Xena	
CLK	I	25MHz clock, as used by Xena	buffer if used
DEBUG	I/O	XMOS debug signal, as used by Xena	
TRST#	I	JTAG test reset	
TCK	I	JTAG test clock	
TMS	I	JTAG test mode select	
TDI	I	JTAG test data in	see note 2
TDO	O	JTAG test data out	see note 2

Table 18: Xorro Slot Signal Descriptions

Notes:

1. Signal direction is with respect to the Xorro card. “I” signifies a signal driven from the motherboard to the card.
2. Cards that do not provide any JTAG devices should connect TDI to TDO, and leave other JTAG signals unconnected.
3. A ‘#’ suffix signifies an active low signal.

Pin	Signal	Signal	Pin
1	n/c	n/c	2
3	TRST#	GND	4
5	XTDI	n/c	6
7	TMS	GND	8
9	TCK	n/c	10
11	DEBUG	GND	12
13	TDO	n/c	14
15	RESET#	GND	16
17	n/c	n/c	18
19	n/c	XTAG#	20

Table 19: XTAG Connector Pinout

Notes:

1. A ‘#’ suffix signifies an active low signal.
2. The XTAG# signal is wired to ground on the XTAG debugger and is used to sense its presence by Nemo (it is pulled up to 3.3V).

8.9 SATA and PATA (IDE)

The pinouts of the 4 SATA port connectors (J3-J6) are shown in Table 20 below. These connectors are labelled “SATA 0” to “SATA 3” respectively.

Pin	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

Table 20: SATA Connector Pinout

The pinout of the PATA (IDE) connector (P6) is shown in Table 21 below. This connector is labelled “IDE”.

Pin	Signal	Signal	Pin
1	RESET#	GND	2
3	DD7	DD8	4
5	DD6	DD9	6
7	DD5	DD10	8
9	DD4	DD11	10
11	DD3	DD12	12
13	DD2	DD13	14
15	DD1	DD14	16
17	DD0	DD15	18
19	GND	(key)	20
21	DMARQ	GND	22
23	IOW#	GND	24
25	IOR#	GND	26
27	IORDY	GND	28
29	DMACK#	GND	30
31	INTRQ	n/c	32
33	DA1	CBLID#	34
35	DA0	DA2	36
37	CS0#	CS1#	38
39	ACTIVE#	GND	40

Table 21: PATA (IDE) Connector Pinout

Note: a '#' suffix signifies an active low signal.

8.10 USB

SB600 USB ports 0 to 7 are taken to standard USB 'A' connectors, positioned at the rear. The pinout of these is shown in Table 22:

Pin	Signal
1	+5V
2	D-
3	D+
4	GND

Table 22: USB A Connector Pinout

Ports 8 and 9 and presented on a header suitable for connection to the system front panel. The pinout of this is shown Table 23:

Pin	Signal	Signal	Pin
1	+5V	+5V	2
3	D-8	D-9	4
5	D+8	D+9	6
7	GND	GND	8
9	(key)	SHEILD	10

Table 23: USB Front Panel Connector Pinout

8.11 Audio

6 of the audio pairs from the codec are wired to a PC99 audio jack connector at the rear. This is suitable for 3.5mm TRS (tip-ring-sleeve) plugs, and is colour coded as shown in Table 24:

Colour	Function
Blue	Line In L/R
Lime	Front L/R (Line Out)
Pink	Mic In L/R
Orange	Centre/LFE
Black	Rear L/R
Silver	Side L/R

Table 24: Rear Panel Audio Connector

2 further pairs are wired to header P16 (labelled FP AUDIO) for connection to the system front panel as shown in Table 25:

Pin	Signal	Signal	Pin
1	MIC IN L	GND	2
3	MIC IN R	PRESENCE#	4
5	HEADPHONE R	SENSE1_RETURN	6
7	SENSE_SEND	(KEY)	8
9	HEADPHONE L	SENSE2_RETURN	10

Table 25: Front Panel Audio Connector Pinout

Note: a '#' suffix signifies an active low signal.

Audio input from a CD drive is supported via header P17 (labelled CD AUDIO) as shown in Table 26:

Pin	Signal
1	L
2	GND
3	GND
4	R

Table 26: CD Audio Connector Pinout

S/P DIF out is provided on header H5 in addition to the TOSlink optical output connector P15 (labelled S/P DIF). S/P DIF in is provided on header P14. H5 and P14 are reserved for factory test. Their pinouts are shown in Table 27 and Table 28:

Pin	Signal
1	GND
2	OUT

Table 27: S/P DIF Out Connector Pinout

Pin	Signal
1	IN
2	GND
3	+3.3V

Table 28: S/P DIF In Connector Pinout

8.12 PLD

The pinout for H2 (labelled PLD JTAG) is shown in Table 29 below:

Pin	Signal	Signal	Pin
1	GND	+3.3V	2
3	GND	TMS	4
5	GND	TCK	6
7	GND	TDO	8
9	GND	TDI	10
11	GND	n/c	12
13	GND	n/c	14

Table 29: PLD JTAG Header

8.13 COP

The pinout for H4 (labelled COP) is shown in Table 30 below:

Pin	Signal	Signal	Pin
1	TDO	n/c	2
3	TDI	TRST#	4
5	n/c	+3.3V	6
7	TCK	n/c	8
9	TMS	n/c	10
11	(pull-up)	n/c	12
13	SRESET#	n/c	14
15	n/c	GND	16

Table 30: COP (Debug) Header

Note: a '#' suffix signifies an active low signal.

8.14 Battery

BAT1 is a coin cell holder, suitable for a CR2032 3V coin cell. Please ensure that the battery orientation is correct when fitting a battery.

Incorrect battery orientation will cause permanent damage to the SB600!

8.15 Fans

3 fan headers provided around the board. P34 is reserved for the CPU fan. P40 and P41 may be used for case fans. The pinout of these is shown in Table 31:

Pin	Signal
1	GND
2	+12V
3	TACHO

Table 31: Fan Header Pinout

Note: the TACHO pin is unconnected on P40 and P41.

8.16 Power

The system PSU should be connected to J2 (labelled ATX POWER), a 24 pin ATX 2.3 power inlet connector with the pinout shown in Table 32:

Pin	Signal	Signal	Pin
1	+3.3V	+3.3V	13
2	+3.3V	-12V	14
3	GND	GND	15
4	+5V	PS_ON#	16
5	GND	GND	17
6	+5V	GND	18
7	GND	GND	19
8	PWR_OK	n/c	20
9	+5VSB	+5V	21
10	+12V	+5V	22
11	+12V	+5V	23
12	+3.3V	GND	24

Table 32: ATX Power Connector

9 AmigaOne X1000 Nemo 2.1 Motherboard Layout Diagram